In the Specification

Please make the paragraph substitutions indicated below. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs.

The sub-title on page 1, line 5 is amended as follows: Technical Field ~~of the Invention~~

The paragraph beginning on page 1, line 7 is amended as follows:

The subject matter ~~present invention~~ relates generally to the field of semiconductors and, more particularly, to improved apparatus and methods for testing memory elements on integrated circuits.

The sub-title on page 1, line 11 is amended as follows: Background Information ~~of the Invention~~

The paragraph beginning on page 2, line 8 is amended as follows:

In testing memory circuits, it is known to employ a type of testing referred to as programmable built-in self-test (PBIST), as described for example in U. S. Pat. No. 5,640,509, assigned to the assignee of the present application ~~invention~~. According to one embodiment of U. S. Pat. No. 5,640,509, a PBIST circuit is provided as part of an IC that also includes a memory circuit. The PBIST circuit comprises a set of programmable registers that determine a test sequence to be performed on the memory circuit.

The sub-title on page 3, line 15 is amended as follows: Detailed Description ~~of Embodiments of the Invention~~

The paragraph beginning on page 3, line 17 is amended as follows:

In the following detailed description of embodiments of the subject matter ~~invention~~, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the subject matter ~~inventions~~ may be practiced. These embodiments are described in sufficient detail to enable

those skilled in the art to practice the subject matter ~~invention~~, and it is to be understood that other embodiments may be utilized and that logical, mechanical, and electrical changes may be made without departing from the spirit and scope of the subject matter ~~present inventions~~. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of embodiments of the subject matter ~~present invention~~ is defined only by the appended claims.

The paragraph beginning on page 3, line 26 is amended as follows:

The subject matter ~~present invention~~ provides a solution to the relatively large amount of silicon area that was required to implement prior art PBIST circuits for testing memory circuits. Various embodiments are illustrated and described herein. In one embodiment, rather than saving all data subsequent to the first detection of a memory failure, the command, address, and program counter values are saved corresponding to the instruction generating the first memory failure as well as to several subsequent instructions. However, only a single memory block of data values is saved. The silicon area of the elements that store the command, address, and program counter values is significantly less than that required to save all data corresponding to the first and subsequent faulty read operations. Methods of operation, as well as application of the apparatus to an electronic assembly, an electronic system, and a data processing system, are also described.

The paragraph beginning on page 4, line 7 is amended as follows:

In addition to the foregoing advantages, the improved memory testing apparatus and methods of the subject matter ~~present invention~~ can be utilized in one embodiment while the memory circuit under test is operated at full operational speed. This is important in order to detect any memory circuit failures that occur only at full operational speed.

The paragraph beginning on page 5, line 18 is amended as follows:

FIG. 3 is a block diagram of an electronic system 50 incorporating at least one electronic assembly 54 with an improved memory testing apparatus in accordance with one embodiment of the invention. Electronic system 50 is merely one example of an electronic system in which the subject matter ~~present invention~~ can be used. In this example, electronic system 50 is a data

processing system that includes a system bus 52 to couple the various components of the system. System bus 52 provides communications links among the various components of the electronic system 50 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

The paragraph beginning on page 10, line 8 is amended as follows:

In 158, set "i" of data values is transferred (e.g. by shifting) out of the data capture flip-flops 106. Typically, these data values are transferred to an additional memory, which is coupled by a suitable bus to the data capture flip-flops 106, and which resides on a different integrated circuit than the memory circuit being tested. For example, they could be stored in main memory 62 (FIG. 3). However, embodiments of the subject matter are ~~invention is~~ not limited to architectures wherein the other memory is located on a different integrated circuit than the memory being tested.

The paragraph beginning on page 11, line 9 is amended as follows:

In 176, set "1" of data values is transferred out of the data capture flip-flops 106. Again, these data values are typically transferred to a memory residing on a different integrated circuit than the memory circuit being tested. For example, they could be stored in main memory 62 (FIG. 3). However, embodiments of the subject matter are ~~invention is~~ not limited to architectures wherein the other memory is located on a different integrated circuit than the memory being tested.

Delete the sub-title "Conclusion" on page 12, line 13.

The paragraph beginning on page 12, line 15 is amended as follows:

The subject matter ~~present invention~~ provides for improved apparatus and methods for fault isolation in memory circuits. In one embodiment, a memory circuit to be tested forms part of a first integrated circuit that further includes at least a processor circuit. Various structures are also fabricated on the first integrated circuit for testing the memory circuit. These structures include storage elements for capturing and storing command, address, program counter, and data

values while minimizing the silicon area used for such storage elements. In addition, an electronic assembly, an electronic system, a data processing system, and various methods of testing a memory have been described. All of these embodiments of the subject matter ~~present invention~~ provide testing, including PBIST testing, of memory circuits while minimizing the silicon area required for the structural elements that implement the memory testing, thus making such embodiments more commercially attractive than known apparatus and methods for performing memory testing.

The paragraph beginning on page 12, line 27 is amended as follows:

As shown herein, the subject matter ~~present invention~~ can be implemented in a number of different embodiments, including an integrated circuit package, an electronic assembly, an electronic system, a data processing system, and various methods for testing memory. Other embodiments will be readily apparent to those of ordinary skill in the art. The elements, architecture, dimensions, and sequence of operations can all be varied to suit particular product and test requirements.

The paragraph beginning on page 13, line 7 is amended as follows:

The various elements depicted in the drawings are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. The drawings are intended to illustrate various implementations of the subject matter ~~invention~~, which can be understood and appropriately carried out by those of ordinary skill in the art.

The paragraph beginning on page 13, line 12 is amended as follows:

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments ~~embodiment~~ shown. This application is intended to cover any adaptations or variations of the subject matter ~~present invention~~. Therefore, it is manifestly intended that embodiments of this subject matter ~~invention~~ be limited only by the claims and the equivalents thereof.